

## REMARKS

Replacement Sheets 1/7 of the drawings, making the corrections required by the examiner in the office action, are enclosed for the examiner's approval. Also, a revised "Abstract of the Disclosure" is enclosed in which the changes required by the examiner have been made.

The examiner has rejected claims 1-14 under 35 U.S.C. § 102 as anticipated by Fasano, U.S. Patent 5,949,030, hereinafter Fasano. This rejection is not thought to be well taken, especially in view of the amendments to claims 1 and 4 and, the only independent claims remaining in the application.

While there are some superficial similarities between Fasano and the instant application, they are directed to solving two distinct and different problems. Fasano states at column 6, lines 5-10:

The present invention allows for fewer holes and holes of a larger diameter to be made in the board through the stiffener to achieve the same I/O density. Subsequent co-axial via connections are made in the dielectric filler within the larger hole. This alleviates manufacturing concerns and reduces costs.

Whereas in the present application the purpose is:

The coaxial via structure can be combined with a stacked via structure so as allow efficient transmission of high speed signals across the electronic device carrier when a manufacturing process limits the creation of a full coaxial via structure across the entire electronic device carrier. (lines 7-11 of body of Abstract)

Thus, as amended, all of the claims require that the surrounding structure be free of signals and the central vias carry the signals. This is not true of the Fasano structure or method. The applicants' method allows the efficient transmission of high speed signals. The instant application addresses the electrical integrity of the signal across many other

### **Amendments to drawing figures**

Please replace sheets 1/7 of the drawings with the attached revised replacement sheets 1/7 of the drawings with the attached revised replacement Sheets 1/7.

layers that are placed above and below the core construction. Structures proposed by the instant application form a complete three dimensional shielding structure that protrudes beyond the "bare core" implementation of what Fasano presents into his patent. Lines are guided into shielded bi-dimensional (in plane) shielding structures (Figure 6) (placed on any given layer not belonging to the core) that are then translated in vertical three-dimensional transmission lines with matched impedance (Figures 7 and 8) including a coaxially made structure embedded in the PCB core. This approach can be applied regardless of the number of layers that the "signal" has to go through and that are built on top (and below for usual symmetry of the construction) of the core section of the PCB (and not exclusively into the core), while in the Fasano application, this is not applicable. In Fasano, the level of structures appears to be limited in the number of coaxially nested structures, and then the signal is surfaced as a not matched (impedance) construction. So the concept of coaxially placed construction is here extended beyond the limited embodiment of the Fasano Patent.

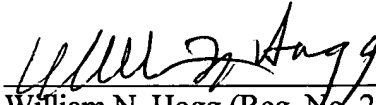
The claims, as amended, clearly define over Fasano wherein it is stated in all of the claims that the central via carries only signals, and the surrounding vias carry no signals, thus allowing efficient and accurate carrying of high speed signals.

In view of the above, it is believed that each of the claims in the application is distinguishable one from the other and over the prior art.

Therefore, reconsideration and allowance of the claims is respectfully requested.

Respectfully submitted,

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William N. Hogg (Reg. No. 20,156)  
Driggs, Lucas, Brubaker & Hogg Co., L.P.A.  
CUSTOMER NO. 26681

WNH:cg

Attachments – Sheets 1/7 of drawings